TITLE OF THE INVENTION

Delay-Compensated Timeslot Assignment Method and System for Point-to-Multipoint Communication Networks

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a packet communication system and a method of assigning timeslots of the system. The present invention is particularly concerned with a dynamic timeslot assignment method for a common medium point-to-multipoint communication system in which multiple local units are connected to a network unit via a common transmission medium and the network unit dynamically assigns timeslots to the local units under varying traffic.

Description of the Related Art

A prior art point-to-multipoint communication system is comprised of a plurality of line concentrators on the user side of the system and a timeslot assignment unit on the network side. Each line concentrator multiplexes (i.e., concentrates) traffic from a plurality of user terminals onto an optical local access line which is coupled by an optical coupler to a common optical line. Each line concentrator includes a buffer for temporarily storing ATM cells received from the associated user terminals and a queue length detector is provided to count the number of outstanding cells in the buffer that form a queue waiting for transmission and sends a queue length signal to the timeslot assignment unit. In order to provide efficient utilization of the common medium for bursty traffic, the timeslot assignment unit dynamically assigns timeslots to the line concentrators based on the queue lengths of the

line concentrators, as disclosed in Japanese Patent Publication 10-242981. According to the prior art timeslot assignment technique, timeslots are assigned to each line concentrator at periodic intervals S as shown in Fig. 1, where the interval S equals to or an integral multiple of the length of a frame. At each assignment time, the timeslot assignment unit determines the number of timeslots to be assigned to each line concentrator during each interval S, and then determines the number of timeslots to be assigned during each frame if the assignment interval S is an integral multiple of the frame length and their position within a frame to produce a slot position signal, which is sent to each line concentrator.

However, there is an inherent control delay in this timeslot assignment process. Specifically, this control delay is a total sum of the intervals for timeslot assignment calculations, the propagation delay time, and the time to establish synchronization with system clock at each side of the network.

As shown in Fig. 1, at time t_0, each line concentrator communicates a queue length signal $Q_0 = 100$ to the timeslot assignment unit 9, indicating that there are one-hundred ATM cells forming a queue in the buffer 6. As long as they remain in the buffer, queue length signals Q_0 will be transmitted at update intervals. Based on a received queue length signal, the timeslot assignment unit 9 calculates the count number G_0 (= 40, for example) of timeslots to be assigned during an assignment period S_0. If the update interval S is equal to the length of a frame, the assignment unit 9 determines the slot positions of assigned timeslots in a frame at time $t_1 - \alpha$ and sends a signal g_{0-i} to the associated line concentrator for indicating the frame-by-frame timeslot count number and the timeslot position (where i indicates

frame number). Timeslot assignment unit 9 successively calculates the numbers of timeslots $G_1 = 50$ and $G_2 = 60$ at times $t_2 - \alpha$ and $t_3 - \alpha$ in response to queue length signals $Q_1 = 100$ and $Q_2 = 100$ and produces timeslot identification signals g_{1-i} and g_{2-i}.

It is seen that the value $G_0 = 40$ produced at time t_0 is actually used by the line concentrator at time t_3 that is delayed by a period of 3S with respect to time t_0. In the same way, the assigned timeslot count numbers $G_1 = 50$ and $G_2 = 60$ produced at times t_1 and t_2 are actually used by the concentrator at times t_4 and t_5. The presence of such control delay implies that there are cells in the buffer 11 which were already assigned timeslots but are still waiting for their turn to be forwarded to the network. For example, at time t_3, there are 100 outstanding cells in the buffer that were already assigned timeslots whose total number equals 150 (= 40 + 50 + 60).

However, because of the delay time fifty timeslots are unnecessarily assigned to the one-hundred outstanding cells. Since the surplus timeslots are not used by the line concentrators, they result in a low throughput in cell transfer. In addition, the delay time associated with the outstanding cells in the buffer and hence the buffer capacity for a given cell loss rate is proportional to the length of the queue. Due to the low cell transfer throughput, there is an increase in cell delay, hence an increase in required buffer capacity.

SUMMARY OF THE INVENTION

It is therefore an object of the present invention to provide a delay-compensated method and system for a packet communication network in which timeslots are not repeatedly assigned to the same packets.

According to a first aspect, the present invention provides a timeslot assignment method for a communication system in which a plurality of end-user systems are connected to a timeslot assignment unit via a common transmission medium, each of the end-user systems comprising a buffer for storing packets of either variable or constant length and forwarding packets from the buffer on assigned timeslots, the method comprising the steps of (a) determining a first count number of said packets in the buffer of each end-user system, (b) determining a second, total count number of timeslots previously assigned to each end-user system during a delay time period of the timeslot assignment unit, (c) using said first and second count numbers for determining a third count number of packets in said buffer to which timeslots are not assigned, and (d) assigning timeslots to packets of each end-user system based on said third count number.

According to a second aspect of the present invention, there is provided a communication system comprising a plurality of end-user systems and a timeslot assignment unit connected via a common transmission medium to the end-user systems. Each of the end-user systems comprises a buffer for storing packets of either variable or constant length, a queue length detector for detecting a queue length indicating a count number of said packets in the buffer, and a controller for forwarding packets from the buffer on timeslots assigned by the timeslot assignment unit and transmitting a signal to the timeslot assignment unit for indicating the detected queue length. The timeslot assignment unit comprises a timeslot count table having a plurality of entries corresponding to the end-user systems. Each of the entries has a length corresponding to a delay time period of the timeslot assignment unit for storing a plurality of count numbers of assigned

timeslots. The timeslot assignment unit (a) determines a total value of count numbers stored in each entry of the timeslot count table, (b) receives the queue length indicating signal from each end-user system, (c) uses the total count number and the received queue length to determine a virtual queue length of each end-user system indicating a count number of packets in the buffer to which timeslots are still not assigned, (d) assigns timeslots to each end-user system based on the virtual queue length, and (e) stores a count number of the assigned timeslots in an entry of the timeslot count table corresponding to each end-user system.

According to a third aspect, the present invention provides a communication system comprising a plurality of end-user systems, and a timeslot assignment unit connected via a common transmission medium to the end-user systems. Each of the end-user systems comprises a buffer for storing packets of either variable or constant length, a queue length detector for detecting a queue length indicating a count number of said packets in the buffer, a memory having a length corresponding to a delay time of said timeslot assignment unit for storing a plurality of count numbers of assigned timeslots, and a controller. The controller directs the buffer to forward packets on timeslots assigned by the timeslot assignment unit, determines a total value of the count numbers stored in the memory, determines from the total value and the queue length a virtual queue length indicating a count number of packets in the buffer to which timeslots are still not assigned. The controller transmits a signal to said timeslot assignment unit for indicating the virtual queue length. The timeslot assignment unit receives the virtual queue length indicating signal from each end-user system and assigns timeslots to each end-user system based on the received virtual queue length.

BRIEF DESCRIPTION OF THE DRAWIGNS

The present invention will be described in detail further with reference to the following drawings, in which:

Fig. 1 is a timing diagram of a prior art slot assignment method;

Fig. 2 is a block diagram of an point-to-multipoint communication system according to a first embodiment of the present invention;

Fig. 3 is a block diagram of the timeslot assignment unit according to the first embodiment of the present invention;

Fig. 4 is a flowchart of the operation of the control logic of Fig. 3;

Fig. 5 is a flowchart of a first form of the timeslot assignment subroutine of Fig. 4;

Fig. 6 is a flowchart of a second form of the timeslot assignment subroutine;

Fig. 7 is a flowchart of a third form of the timeslot assignment subroutine;

Fig. 8 is a view for illustrating the operation of the assignment subroutine of Fig. 7;

Fig. 9 is a timing diagram for illustrating the operation of the present invention;

Fig. 10 is a block diagram of a communication system according to a modified embodiment of the present invention;

Fig. 11 is a block diagram of the timeslot assignment unit of Fig. 10;

Fig. 12 is a flowchart of the operation of the line concentrators of Fig. 10; and

Fig. 13 is a flowchart of the operation of the first control logic of Fig.

11.

DETAILED DESCRIPTION

Referring now to Fig. 2, there is shown an ATM-PON (asynchronous transfer mode-passive optical network) system, or a point-to-multipoint communication system according to a first embodiment of the present invention. On the user side of the system, end-user systems, or line concentrators 1 of identical configuration are located at or near user terminals 2 to multiplex (i.e., concentrate) their traffic to each of a plurality of optical local access lines 3, which are connected by an optical coupler 4 to a common optical transmission medium 5. Each line concentrator includes a buffer 6 for temporarily storing ATM cells received via a line interface 9 from the associated user terminals 2. A queue length detector 7 is connected to the buffer 6 to determine the number of cells that form a queue in the buffer waiting for transmission and communicates the queue length to the network. A timing controller 8 is provided in each line concentrator for controlling the buffer 6 to forward a cell on an assigned timeslot and the queue length detector 7 to transmit a queue length signal. A line interface 10 is provided for converting electrical signals from buffer 6 and detector 7 to corresponding optical signals for transmission to the access line 3.

On the network side, the transmission medium 5 is connected to a switching office of a switched communication network, not shown, via an optical splitter 12. A timeslot assignment unit 13 is connected to the transmission medium 5 to receive queue length signals from all line concentrators 1 via optical splitter 12 to provide timeslot assignment and sends timeslot position signals destined for respective line concentrators 1.

These signals are sent via a common optical signaling line 14 and an optical splitter 15 to local optical signaling lines 16 to the line concentrators 1 for indicating the positions of respectively assigned timeslots within the interval of a frame.

In response to a timeslot position signal, the timing controller 8 of each line concentrator 1 directs the buffer 6 to forward an ATM cell on the assigned timeslot so that no data collisions occur on the common medium 5.

In addition, the time slot assignment unit 13 transmits a timing signal at periodic intervals to all line concentrators. In response to a timing signal, the timing controller 8 of each line concentrator 1 directs the queue length detector 7 to send its output to the timeslot assignment unit 13.

As shown in detail in Fig. 3, the timeslot assignment unit 13 is comprised of a first control logic 30, a queue length table 31, a timeslot count table 32 and a second control logic 34. First control logic 30 receives queue length signals from the line concentrators 1 via a line interface 33. Queue length table 31 is segmented into a plurality of entries corresponding to the line concentrators. First control logic 30 stores the queue length values of the received signals into corresponding entries of queue length table 31. Timeslot count table 32 is also segmented into a plurality of entries corresponding to the line concentrators. Each entry of the timeslot count table 32 is sub-divided into a number of fields corresponding to "k" assignment update intervals $t_j - t_{j+1}$ to $t_{j+k-1} - t_{j+k}$, where j represents the current time interval. The time interval between t_j to t_{j+k} represents the delay time which the second control logic 34 usually takes to process and transmit timeslot position signals plus the propagation delay time between the timeslot assignment unit

and the line concentrators and their data processing times, and so on. As will be described, the first control logic 30 stores a count number of timeslots assigned to a given line concentrator during a given update interval into a field of the timeslot count table 32 that corresponds to the given line concentrator and the given time interval. Timeslot count table 32 is therefore a past record of assigned timeslot count numbers over "k" update intervals. Then, the control logic 30 supplies the count number of timeslots assigned to each line concentrator to the second control logic 34, which determines the positions of assigned timeslots within a frame and transmits a signal representing the timeslot positions to each line concentrator via a line interface 35 and the common signaling line 14. Second control logic 34 also functions to transmit a timing signal to the line concentrators via the signaling line at periodic intervals corresponding to update intervals of the first control logic 30 in order to urge the line concentrators to return a queue length signal.

The operation of first control logic 30 proceeds according to the flowcharts shown in Figs. 4 to 7.

In Fig. 4, the control logic 30 monitors a timing source, not shown, for updating assigned timeslots at step 401. In response to a timing pulse, the control logic 30 proceeds to step 402 to receive queue length signals on predetermined timeslots from the line concentrators indicating the queue lengths of their outstanding cells and stores the queue length values into corresponding entries of the queue length table 31.

At step 403, a variable "i" is set equal to one, where "i" identifies a line concentrator. Control logic 30 then reads all timeslot count numbers from the

entry "i" of timeslot count table 32 and calculate the total number Ni of timeslots assigned to the line concentrator "i" during previous "k" update intervals (step 404).

Control logic 30 reads the queue length value Qi from the entry "i" of queue length table 31 (step 405) and calculates the difference between Qi and Ni as a "virtual" queue-length VQi of the line concentrator "i" (step 406). Steps 404 to 406 are repeated to produce virtual queue-lengths for all line concentrators by incrementing the variable "i" (step 408) until it equals the number of all line concentrators represented by the integer L (step 407).

Next, the control logic 30 performs a timeslot assignment subroutine 410. As described in detail, the control logic 30 assigns timeslots according to an algorithm and determines the number of timeslots (Ci) assigned to each line concentrator as will be described in Figs. 5, 6 and 7 based on the virtual queue length values of the line concentrators.

At step 411, the first control logic 30 supplies the number of timeslots assigned to each line concentrator to the second control logic 34. The latter determines the positions of the assigned timeslots within a frame and transmits signals each representing the timeslot positions to the line concentrators over the common signaling medium 14. At step 412, all contents of timeslot count table 32 are shifted by one column so that the oldest data are deleted and a new column of fields is vacated for storing the timeslot count numbers Ci as most recent timeslot count values. Control logic 30 now returns to the starting point of the routine.

Fig. 5 illustrates one embodiment of timeslot assignment subroutine 410 in which timeslots are assigned on a round-robin basis. At step 501, the

control logic 30 determines the number of available timeslots (A) that can be assigned.

At step 502, the variable "i" is set equal to one and a count value Ci of the line concentrator "i" is set equal to zero. Decision step 503 is then executed by checking to see if the virtual queue length VQi of the line concentrator "i" is zero. If VQi is positive, the decision at step 503 is negative and the control logic assigns one timeslot to line concentrator "i" at step 504. At step 505, the available timeslot number A is decremented by one and the count value Ci is incremented by one. If VQi is zero, the control logic assigns no timeslots and skips steps 504 and 505. By incrementing the variable "i", round-robin assignment steps 503 to 505 will be repeated until the available timeslots reduce to zero (steps 506, 507). Therefore, timeslots are assigned on a round-robin basis to those line concentrators whose virtual queue lengths are positive.

In Fig. 6, the control logic 30 assigns timeslots to each line concentrator by an amount proportional to its virtual queue length. When the available timeslots A is determined (step 601), a total value S of virtual queue lengths VQi of all line concentrators is calculated (step 602). Variable "i" is set equal to 1 (step 603) and the VQi value is tested (step 604) to see if it is positive or zero. If VQi is positive, flow proceeds to step 605 to calculate a count number of timeslots $Ci = A \times VQi/S$. Control logic 30 assigns Ci timeslots to line concentrator "i" (step 606). If VQi is zero, the control logic assigns no timeslots and skips steps 605 and 606. By incrementing the variable "i", assignment steps 604 to 606 will be repeated until all line concentrators are tested (steps 607, 608).

In Fig. 7, the control logic 30 assigns timeslots such that the virtual queue lengths of all line concentrators will be averaged out. Initially, the control logic 30 determines the number of available timeslots (A) at step 701, arranges the VQ values in descending order (step 702) and sets a variable "h" to one, with h = 1 representing the highest of the VQ values. At step 704, the difference between VQ_h and $VQ_{(h+1)}$ is determined as a count number C_h of timeslots to be assigned. At step 705, the control logic determines whether the number of available timeslots is equal to or greater than a total number of timeslots to be assigned which equals $h \times C_h$. If $A \geq h \times C_h$, flow proceeds from step 705 to 706 to assign C_h timeslots to "h" line concentrators of higher VQ values. If $A \leq h \times C_h$, the count number C_h is set equal to A/h at step 707 and flow proceeds to step 706 to assign A/h timeslots to the "h" line concentrators. At step 708, the available timeslot count number A is decreased by the number of assigned timeslots C_h in order to update its value as a remaining timeslot resource. Decision step 709 then determines whether the remaining resource A is equal to or smaller than the smallest of the VQ values. If the decision at step 709 is negative, the variable "h" is incremented by one (step 710) and the routine returns to step 704 to repeat the assignment process on the line concentrator of next highest VQ value. If the remaining resource A is smaller than the smallest of the VQ values, decision step 711 is executed to determine the total number Ci of timeslots assigned to each line concentrator.

For example, assume that the number of available timeslots is initially 90 and line concentrators 1a, 1b, 1c, 1d and 1e have virtual queue length values 20, 50, 40, 40 and 10, respectively, as shown in Fig. 8. Thus, the

following timeslots are assigned:

When $h = 1$, $C_1 = 50 - 40 = 10$ assigned to concentrator 1b,

When $h = 2$, $C_2 = 40 - 40 = 0$ (no timeslots are assigned),

When $h = 3$, $C_3 = 3 \times (40 - 20) = 60$ assigned to concentrators 1b, 1c, 1d,

When $h = 4$, $C_4 = 4 \times 20/4 = 20$ assigned to concentrators 1a, 1b, 1c, 1d.

In this way, VQ values are averaged out and their variability among the line concentrators is reduced. Therefore, each line concentrator is not required to maintain a buffer of large storage capacity.

The operation of a line concentrator of the present invention will be understood by the following description with reference to a time sequence diagram shown in Fig. 9.

Assume that the line concentrator has a queue length value 100 at update times t_0, t_1 and t_2. First control logic 30 initially determines that virtual queue length (VQ) value is equal to 100. Since no timeslots are assigned during the first interval t_0 to t_1, 40 timeslots may be assigned to the line concentrator at time $t_1 - \alpha$. The VQ value of the concentrator at time t_1 thus equals 60. Using this VQ value which is smaller than the original VQ value of 100, the control logic 30 may assign a smaller number of timeslots, 35, for example, at time $t_2 - \alpha$, resulting in a VQ = 25 at time t_2. With VQ = 25, the control logic may assign 25 timeslots and transmits at $t_3 - \alpha$, leaving a VQ = 0 at time t_3. The count numbers 40, 35 and 25 of assigned timeslots are respectively supplied to the second control logic 34 at times $t_1 - \alpha$, $t_2 - \alpha$, and $t_3 - \alpha$. Due to the inherent delay time involved with the timeslot position calculation, the second control logic 34 produces a timeslot position signal $g_{0\text{-}i}$ at time $t_3 - \alpha$ in response to the assigned slot count number = 40

following a delay time of two update intervals. However, the total number of timeslots assigned to the line concentrator at time t_3 equals the queue length value of 100. Thus, timeslots are not repeatedly assigned to the same outstanding cells.

A modified embodiment of the present invention is shown in Figs. 10 to 13. This embodiment differs from the previous embodiment in that each of the line concentrators has a controller 20, a timeslot count memory 21 and a queue length detector 22, as shown in Fig. 10. Controller 20 of each line concentrator determines its own virtual queue length by using data stored in the timeslot count memory 21 and the output of the queue length detector 22 and informs the timeslot assignment unit 13A of the VQ value. Similar to each entry of the timeslot count table 32, the timeslot count memory 21 stores a count number of timeslots assigned during an update interval $t_j - t_{j+1}$ into one of its fields.

On the other hand, the timeslot assignment unit 13A shown in Fig. 11 is similar to the previous embodiment with the exception that the tables 31 and 32 of the previous embodiment are dispensed with and the first control logic 30A is associated with the second control logic 34 and the line interface 35.

The operation of the controller 20 of each line concentrator of Fig. 10 proceeds according to the flowchart of Fig. 12. Controller 20 monitors its local signaling line to detect a broadcast timing signal and an assigned slot count and a timeslot position signal that are addressed to its own line concentrator (steps 801, 802 and 803). If a timeslot position signal is received (step 803), the controller 20 directs the buffer 6 to transmit cells on the

timeslots specified by the position signal (step 804) and returns to the starting point of the routine.

If an assigned slot count signal is received (step 802), flow proceeds to step 805 to store the count number contained in the received signal into the timeslot count memory 21 and returns to the starting point of the routine.

If a timing signal is received (step 801), the controller proceeds to step 806 and reads all timeslot count numbers from the timeslot count memory 21 and calculate a total count number of the assigned timeslots (C). At next step 806, the controller 20 reads a current queue length value (Q) from the queue length detector 22 (step 807) and determines a virtual queue length (VQ) value by subtracting C from the value Q (step 808) and communicates this VQ value to the timeslot assignment unit 13A (step 809). Controller 20 then returns to the starting point of the routine.

The operation of the first control logic 30A of Fig. 11 proceeds according to the flowchart of Fig. 13. Control logic 30A receives VQ signals and count numbers from the line concentrators (step 901). By using the VQ values from the line concentrators, the control logic 30A executes timeslot assignment subroutine 902 in a manner as described previously and determines a count number Ci of timeslots assigned to a line concentrator "i". At step 903, the first control logic 30A communicates the assigned-timeslot count numbers respectively to all line concentrators via the line interface 35 and communicates the same information to the second control logic 34 for timeslot position calculation and transmission of position signals to the line concentrators.

While mention has been made of embodiments in which ATM cells

(packets of constant length) are discussed, the present invention could also be applied to a communication system in which packets of variable length are used. In such instances, packet length information is transmitted from the line concentrators to the timeslot assignment unit to determine the number of timeslots to be assigned to outstanding packets in the line concentrators.